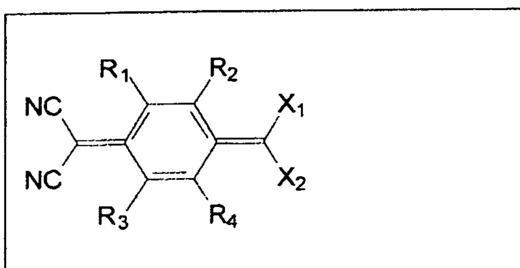
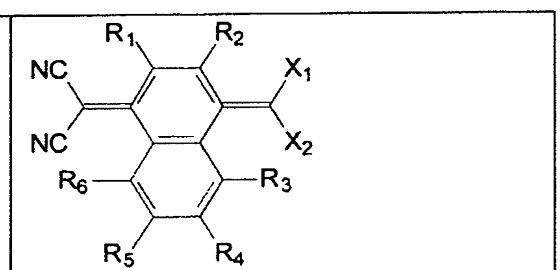
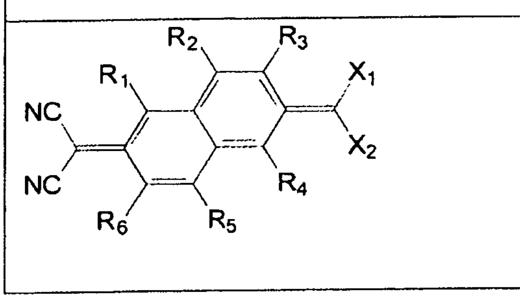
Patent claims

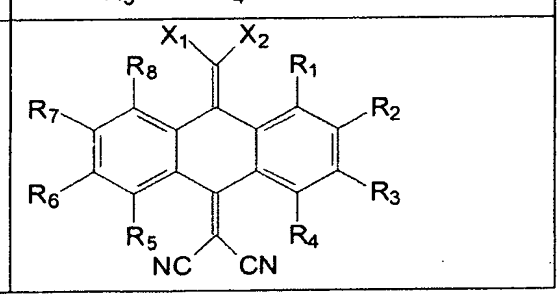
1. A semiconductor arrangement having at least one nonvolatile memory cell which has a first electrode comprising at least two layers and has an organic material,
the organic material forming a compound with that layer of the first electrode which is in direct contact.

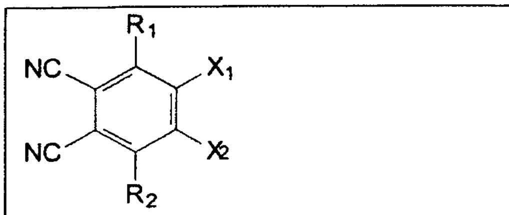
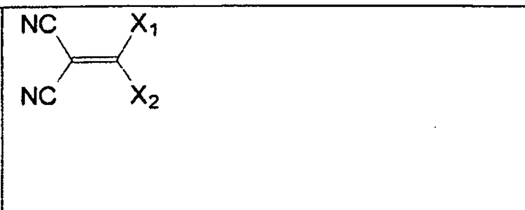
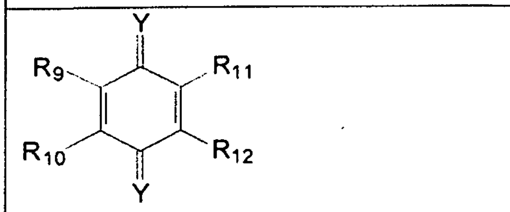
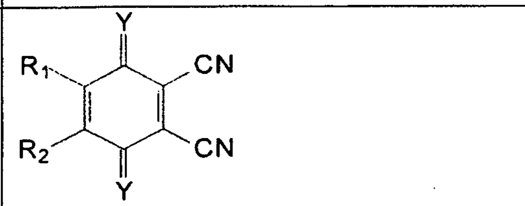
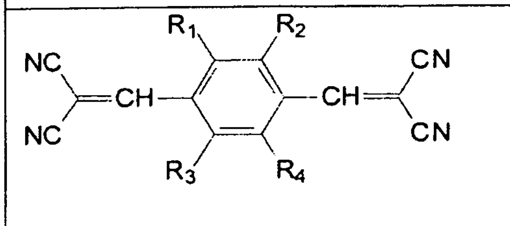
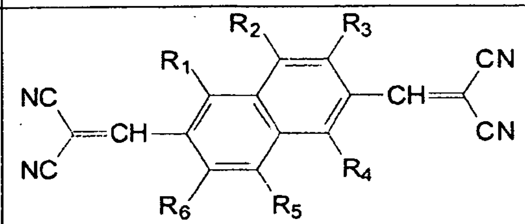
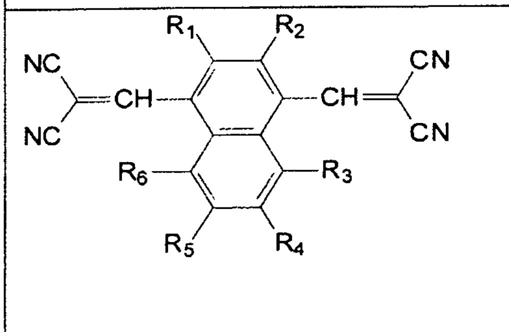
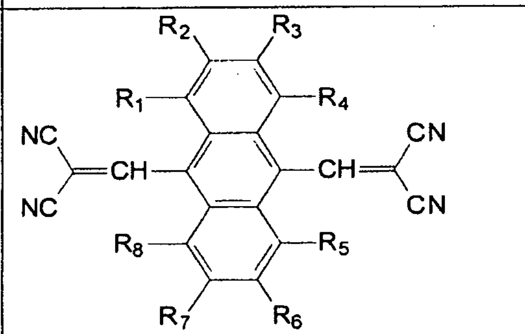
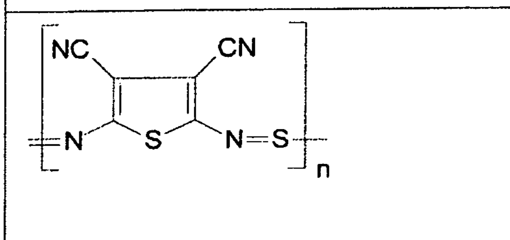
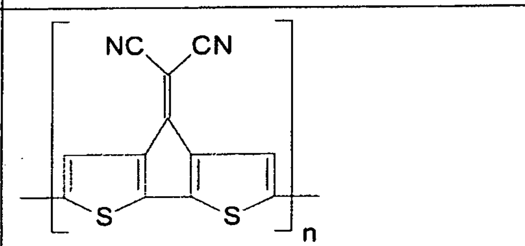
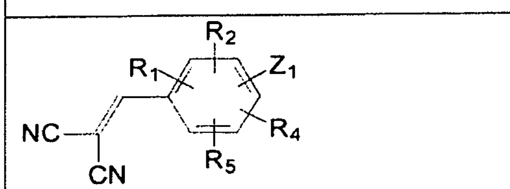
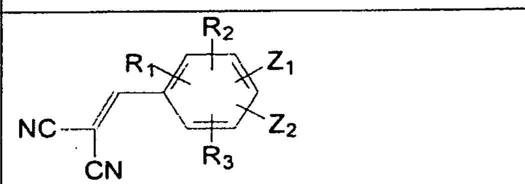
2. The semiconductor arrangement having a nonvolatile memory cell as claimed in claim 1,
wherein
the organic material has at least one of the following materials or compounds: sulfur, selenium or tellurium either in pure or in bonded form in particular as organocompounds of sulfur, selenium or tellurium, and sulfur-, selenium- or tellurium-containing oligomers or polymers, and/or one of the following compounds:

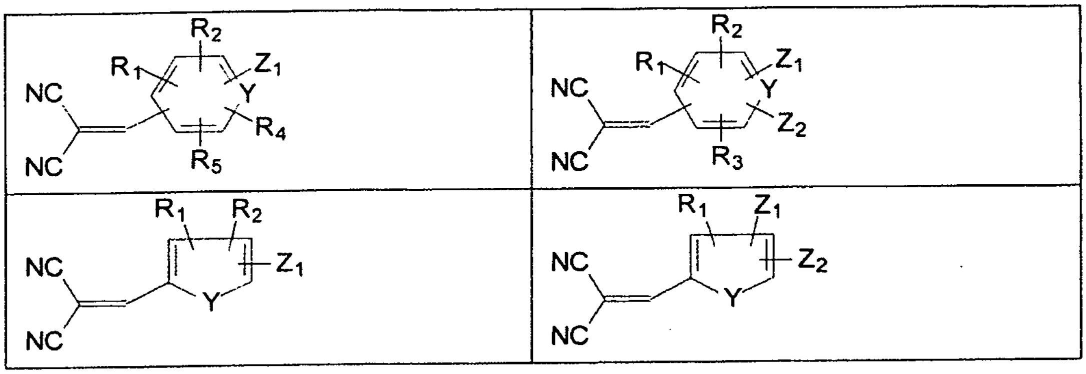




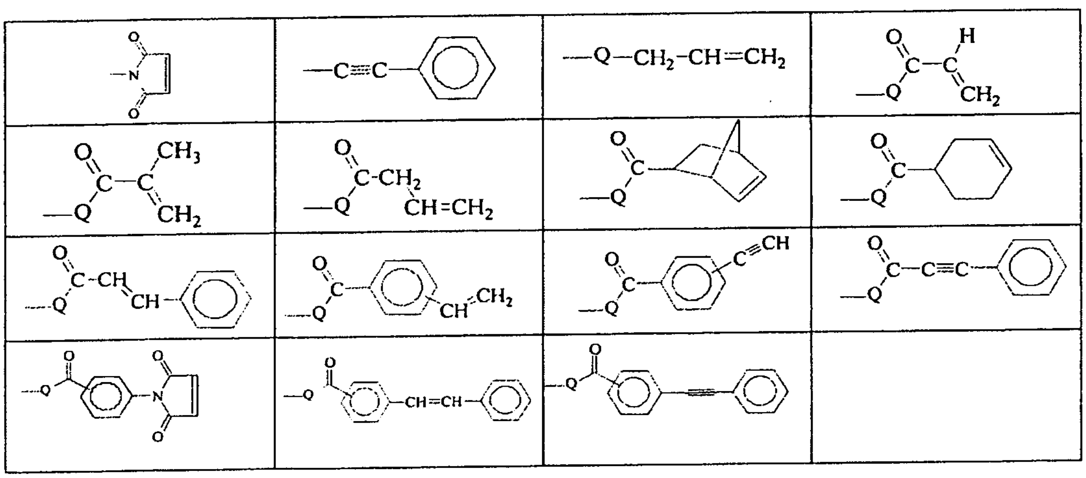






where R_1, R_2, R_3, R_4, R_5, R_6, R_7 and R_8, independently of one another, have the following meaning: H, F, Cl, Br, I (iodine), alkyl, alkenyl, alkynyl, O-alkyl, O-alkenyl, O-alkynyl, S-alkyl, S-alkenyl, S-alkynyl, OH, SH, aryl, heteroaryl, O-aryl, S-aryl, NH-aryl, O-heteroaryl, S-heteroaryl, CN, NO_2, $-(CF_2)_n-CF_3$, $-CF((CF_2)_nCF_3)_2$, $-Q-(CF_2)_n-CF_3$, $-CF(CF_3)_2$, $-C(CF_3)_3$ and



n: n = 0 to 10

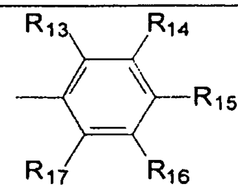
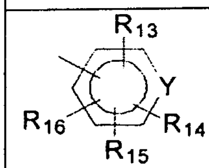
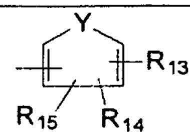
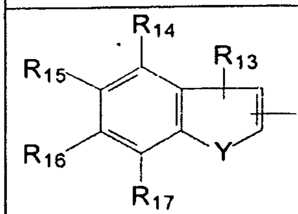
Q: -O-, -S-

R_9, R_{10}, R_{11}, R_{12} may, independently of one another, be: F, Cl, Br, I, CN, NO_2

R_{13}, R_{14}, R_{15}, R_{16}, R_{17} may, independently of one another, be:

H, F, Cl, Br, I, CN, NO_2

X_1 and X_2 may, independently of one another, be:

CN	
	
	

Y is: O, S, Se
and Z_1 and Z_2, independently of one another, are: CN, NO_2.

3. The semiconductor arrangement having a nonvolatile memory cell as claimed in claim 1 or 2,
wherein
the organic material is an electron acceptor.

4. The semiconductor arrangement having a nonvolatile memory cell as claimed in claim 3,
wherein
the electron acceptor has electron-attracting atoms or groups which are selected from: -Cl, -F, -Br, -I, -CN, -CO-, $-NO_2$.

5. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of claims 1 to 4,
wherein

the organic material forms a charge transfer complex with the bottom electrode.

6. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of claims 1 to 5, wherein
that layer of the first electrode which is in contact with the organic material contains copper or silver.

7. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of the preceding claims, wherein
the organic material is present in a film thickness of between 30 and 1000 nm, preferably between 30 and 300 nm.

8. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of the preceding claims, wherein
the cell is scalable up to an area of 40 nm^2.

9. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of the preceding claims, wherein
that layer of the first electrode which is not in contact with the organic material is titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten (W), TiW, TaW, WN, WCN, IrO, RuO, SrRuO, or a combination of said layers and/or materials and, if appropriate, is additionally provided with a layer made of Si, TiNSi, SiON, SiO, SiC or SiCN.

10. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of the preceding claims, wherein
the second electrode is made of aluminum, copper, AlCu, AlSiCu, silver (Ag), titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten

(W), TiW, TaW, WN, WCN, IrO, RuO, SrRuO, or a combination of said layers and/or materials and, if appropriate, is additionally provided with a layer made of Si, TiNSi, SiON, SiO, SiC or SiCN.

11. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of the preceding claims, wherein the cell can be switched between an ON state and an OFF state.

12. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of the preceding claims, wherein the ON and OFF states have different electrical resistances.

13. The semiconductor arrangement having a nonvolatile memory cell as claimed in claim 12, wherein the ratio between the ON and OFF states is more than 66.

14. A method for producing a nonvolatile memory cell as claimed in one of the preceding claims, characterized by the following steps of:

- providing a first electrode, which comprises at least two layers and a layer of the first electrode may form a compound with an organic material;
- contacting the electrode with an organic material in order to form a compound;
- and forming a second electrode on the compound formed.

15. The method for producing a nonvolatile memory cell as claimed in claim 14, wherein

the organic material is vapor-deposited onto the electrode under reduced pressure.

16. The method for producing a nonvolatile memory cell as claimed in claim 14, wherein the organic material is dissolved in a solvent in the process of contacting the first electrode.

17. The method as claimed in one of the preceding claims 14 to 16, wherein the organic material is subjected to a thermal treatment prior to forming the second electrode.

18. The method as claimed in one of claims 14 to 17, wherein prior to forming the second electrode, the excess organic material is rinsed with a solvent.

19. The method as claimed in claim 15, wherein the organic material is vapor-deposited at a pressure of between 0.00001 and 200 mbar.

20. The method as claimed in one of claims 14-19, wherein the contacting of the organic material takes place at a substrate temperature of between -50ºC and 150ºC.

21. The method as claimed in one of claims 14, 15, 17 to 20, wherein the organic material is mixed in the gas phase with a carrier gas.

22. The method as claimed in one of claims 14 to 21, wherein

prior to providing the second electrode, the compound formed is treated with an aftertreatment reagent.

23. The method as claimed in claim 22, wherein the aftertreatment reagent is selected from the following group: amines, amides, ethers, ketones, carboxylic acids, thioethers, esters, aromatics, heteroaromatics, alcohols or sulphur- or selenium-containing compounds.

24. The method as claimed in claim 23, wherein the sulphur-containing compounds are selected from the group containing: sulphur hetercyclic compounds, -SO-containing compounds and thiols.

25. The method as claimed in one of claims 22-24, wherein the aftertreatment reagent is selected from the group containing: diethylamine, triethylamine, dimethylaniline, cyclohexylamine, diphenylamine, dimethylformamide, dimethylacetamide, dimethyl sulfoxide, acetone, diethylketone, diphenylketone, phenyl benzoate, benzofuran, N-methylpyrrolidone, gamma-butyrolactone, toluene, xylene, mesitylene, naphthaline, anthracene, imidazole, oxazole, benzimidazole, benzoxazole, quinoline, quinoxaline, fulvalene, furan, pyrrole, thiophene or diphenyl sulfide.

26. The method as claimed in one of claims 22 to 25, wherein the aftertreatment reagent is present in a solution.

27. The method as claimed in one of claims 22-25, wherein the aftertreatment reagent is present as vapor.

28. The method as claimed in one of claims 22-27, wherein
the aftertreatment time is between 15 seconds and 15 minutes.

29. The method as claimed in one of claims 22 to 28, wherein
the aftertreatment takes place at a temperature of -30ºC to 150ºC.

30. The method as claimed in one of claims 14-21, wherein,
in the process of contacting the first electrode with the organic material, the aftertreatment reagent as claimed in one of claims 22-25 is admixed with the solution containing the organic material or with the vapor containing the organic material.

31. The semiconductor arrangement as claimed in one of claims 1-13,
having the aftertreatment reagent as claimed in one of claims 22-25, and/or a reaction product of the aftertreatment reagent with the organic material and/or the electrode material.

32. The semiconductor arrangement having a bit line and a word line having a nonvolatile memory cell as claimed in one of claims 1-13 and/or 31, the nonvolatile memory cells being situated directly between bit and word lines that cross one another.

33. The semiconductor arrangement as claimed in claim 32,
wherein
the nonvolatile memory cells are present in a plurality of layers.

34. The semiconductor arrangement as claimed in claim 32 or 33,
which can be produced by the following steps in any desired order:

- forming at least one first interconnect on a substrate, which serves as first electrode for the memory cell as claimed in one of claims 1-13 or 31;
- depositing an insulating layer;
- patterning the insulating layer, so that in the insulating layer trenches are patterned for at least one interconnect transversely with respect to the first interconnects applied;
- depositing an organic material as claimed in one of claims 2 to 5;
- depositing at least one second electrode, which is arranged transversely with respect to the first interconnect applied and serves as a second electrode for the memory cell.

35. The semiconductor arrangement as claimed in claim 34,
wherein
the deposition of the insulating layer is effected after the deposition of the organic material.

36. The semiconductor arrangement as claimed in claim 33,
which can be produced by the following steps in this order:

- forming at least one first interconnect on a substrate;
- depositing an insulating layer;
- patterning the contact holes above the first electrode;
- depositing an organic material as claimed in one of claims 2-5 into the contact holes over the first electrode;

- depositing a second insulating layer;
- patterning the second insulating layer, so that in the insulating layer trenches are patterned for at least one second interconnect, which runs transversely with respect to the first interconnects applied and covers the contact holes in the cell array;
- depositing at least one second interconnect, which serves as a second electrode for the memory cell as claimed in one of claims 1-13 and/or 31.

37. The semiconductor arrangement as claimed in one of claims 32 to 34,
wherein
it is produced by a Cu damascene technique.

38. A method for producing a semiconductor arrangement as claimed in one of claims 32-37,
characterized by
- forming at least one first interconnect on a substrate, which serves as first electrode for the memory cell as claimed in one of claims 1-13 and/or 31;
- depositing an insulating layer;
- patterning the insulating layer, so that in the insulating layer trenches are patterned for at least one interconnect transversely with respect to the first interconnects applied;
- depositing an organic material as claimed in one of claims 2-5;
- depositing at least one second electrode, which is arranged transversely with respect to the first interconnect applied and serves as a second electrode for the memory cell as claimed in one of claims 1-13 and/or 31.

39. The method as claimed in claim 38,
wherein

the deposition of the insulating layer is effected after the deposition of the organic material.

40. A method for producing a semiconductor arrangement as claimed in one of claims 32-37,
characterized by

- applying at least one first interconnect on a substrate;
- depositing an insulating layer;
- patterning the contact holes above the first electrode;
- depositing an organic material as claimed in one of claims 2-5 into the contact holes over the first electrode;
- depositing a second insulating layer;
- patterning the second insulating layer, so that in the insulating layer trenches are patterned for at least one second interconnect, which runs transversely with respect to the first interconnects applied and covers the contact holes in the cell array;
- depositing at least one second interconnect, which serves as a second electrode for the memory cell as claimed in one of claims 1-13 and/or 31.

41. The method as claimed in one of claims 38-40,
wherein
after the deposition of the organic material, a protective layer is deposited on the organic material prior to further processing.

42. A memory device containing a plurality of the nonvolatile memory cells as claimed in one of claims 1-13 and/or 31.

43. The memory device as claimed in claim 39,
wherein
a plurality of memory cells are arranged in one plane.

44. The memory device as claimed in claim 42 or 43, wherein
a plurality of memory cells as claimed in one of claims 1 to 13 and/or 31 are arranged in the XY plane and in the XZ or YZ plane.